Refine Search

10/673,539

Search Results -

Terms	Documents
L6 and DMOS	1

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
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EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L7

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, October 18, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=ADJ		
L7	L6 and DMOS	1	L7
L6	L5 and (second near3 (drain))	54	L6
L5	L4 and gate and (n adj type) and (p adj type)	103	L5
L4	L3 and (second adj conductivity)	134	L4
L3	L2 and (silicide)	499	L3
L2	L1 and (upper adj surface)	1189	L2
L1	(mos adj device)	7828	L1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 1 of 1 returned.

1. Document ID: US 6600182 B2

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L7: Entry 1 of 1                File: USPT                    Jul 29, 2003

US-PAT-NO: 6600182
DOCUMENT-IDENTIFIER: US 6600182 B2

TITLE: High current field-effect transistor
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Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

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Terms	Documents
L6 and DMOS	1

Display Format: TI Change Format

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L7: Entry 1 of 1 File: USPT Jul 29, 2003

DOCUMENT-IDENTIFIER: US 6600182 B2
TITLE: High current field-effect transistor

Abstract Text (1):
A MOSFET that provides high current conduction at high frequency includes a deposited layer over a substrate of a first conductivity type, with source and drain regions adjoining a top surface of the epitaxial layer. The drain region has a first portion that extends vertically through the epitaxial layer to connect to the substrate and a second portion that extends laterally along the top surface. A first region is disposed in the epitaxial layer between the extended region and the source region. An insulated gate is located above the first region between the source region and the second portion of the drain region. A drain metal layer contacts a bottom surface of the substrate, and a source metal layer that substantially covers the top surface connect to the source region.

Brief Summary Text (5):
One of the problems, however, with these trench devices is that they suffer from increased gate capacitance and Miller capacitance, which negatively affects device operation at high frequencies. This results in a proportional increase in the switching (AC) power losses at high frequency.

Brief Summary Text (6):
Lateral MOSFET devices have a much lower drain-to-gate overlapping and therefore a much lower Miller capacitance as compared with vertical devices. In general, lateral devices also have a comparable on-state resistance to that of vertical structures, but with lower parasitic capacitance values. Hence, lateral MOSFETS are usually better suited for high frequency operations. For instance, lateral MOSFETs are commonly used in RF and microwave amplifiers operating in the gigahertz (GHz) frequency range. Examples of traditional lateral MOSFET device structures for power applications include U.S. Pat. Nos. 5,869,875, 5,821,144, 5,760,440, and 4,748,936.

Brief Summary Text (7):
Traditionally designed lateral MOSFETs have a P+ region near the source, often called a sinker. The purpose of the sinker is to provide a good contact to the P-body region under the source for more efficient hole collection. This relatively deep P+ region protrudes through the epitaxial region and reaches into the P+ substrate. U.S. Pat. Nos. 5,869,875 and 5,821,144 teach replacing the relatively wide P+ sinker diffusion in a traditional DMOS structure with either a conducting trench or a partial trench with a P+ sinker diffusion region. The result is a smaller cell size and lower on resistance. However, the drain electrode structure limits the current conduction capability in these structures, since current flows only through narrow metal drain strips.

Brief Summary Text (8):
U.S. Pat. No. 4,748,936 also discloses a MOS device with a trench in the epitaxial layer that also suffers from drain current flow through the metal formed of stripes to the appropriate wire bonding area. In this approach, like the others described

above, improvement in the lateral device relates to cell area reduction. This area reduction is achieved by replacing the diffused sinker area (that consumes a lot of area connecting the source to the substrate) with an etched trench structure. One of the chief drawbacks, however, of the aforementioned device structures is that they do not provide for adequate high current conduction.

Brief Summary Text (9):
The device structure taught in U.S. Pat. No. 5,760,440 does provide improved current conduction in a lateral MOSFET transistor; however, the teaching of this patent is limited to n-channel transistors having a N+ substrate and a P-type epitaxial structure. As a result, the P-type epitaxial region is not effectively connected to the source region and there is a problem with hole extraction from the P-body under the source. One consequence of this is that the device structure suffers from weak safe operating area (SOA) performance level and poor reliability.

Detailed Description Text (3):
FIG. 1 is a cross-sectional side view of a conventional power MOSFET that includes a trench gate 107 insulated from the semiconductor substrate by oxide layer 108. Gate 107 extends down through p-type layer 105 into n-type layer 104, which is disposed above N+ drain region 103. Source regions 109 adjoin gate 107 at the upper surface of the substrate. Current flows vertically from source electrode 101, into source regions 109, down through the channel regions formed adjacent to the gate 107, across extended drain region 104 and drain region 103, to drain electrode 102.

Detailed Description Text (4):
Although current is efficiently transferred through the metalized top and bottom electrodes in the transistor of FIG. 1, the capacitance formed between the trench gate 107 and silicon regions 104 and 105 negatively affects device performance at high frequencies. Basically, this capacitance causes an increase in switching power losses that is proportional to the frequency of operation. For this reason, practitioners in the semiconductor arts have generally preferred lateral device structures for high frequency power applications. However, as previously discussed the drawback of prior art lateral MOSFET power devices is either their inability to provide efficient current conduction or their safe operating area (SOA) weakness when high current and high voltage are simultaneously applied.

Detailed Description Text (6):
The device of FIG. 2 comprises a MOSFET 10 having a gate 23 (comprised, for example, of polysilicon), and a gate-Insulating layer 24 that insulates gate 23 from the underlying semiconductor regions. Gate-insulating layer 24 may comprise ordinary silicon dioxide or another appropriate dielectric insulating material. In one embodiment gate 23 comprises polysilicon formed with a silicide top layer to reduce gate resistance. The gate is about 1 micron long and insulating layer 24 is approximately 300-500 angstroms thick.

Detailed Description Text (8):
A P-type region 14 is shown formed in P-type semiconductor (e.g., epitaxial) layer 12 separating extended drain region 15 from source region 17. Region 14 prevents punch-through between the source and drain. P-type region 14 also controls the threshold voltage of the transistor and prevents the parasitic NPN bipolar transistor from turning on. By way of example, P-type region 14 may be formed with a diffusion of implanted boron impurities of about 1.times.10.sup.14 cm.sup.-2.

Detailed Description Text (9):
Note that gate 23 slightly overlaps N+ Source region 17 and the extended drain region 15 to provide continuous conduction in the channel region of the device. The overlap with region 14 also enables higher breakdown voltage of the device. However, the overlap between layers 14 & 15 is not required for the device

operation. The channel region of MOSFET 10 is defined at one end by N+ source region 17 and at the other end by N-type extended drain region 15. A channel of electrons is formed along the surface of P-type region 14 just below gate 23 when the MOSFET device is turned on by application of a sufficient voltage to the gate. The thickness of gate insulating layer 24 is made sufficiently large (300-500 angatroms) to avoid high gate capacitance, thereby providing good high frequency performance. Epitaxial layer 12 is formed on top of a P+ substrate 11. To achieve a desired breakdown voltage in the device structure of FIG. 2 the charge in layer 12 is balanced and optimized for highest breakdown voltage (BVD) and lowest Rds(on). In the example of FIG. 2, the optimized resistance of the extended drain region 15 is in the range of 1500-2500 ohm/sq. The epitaxial layer is doped to a concentration of about 1.times.10.sup.16 cm.sup.-3 is fabricated to be about 3 microns thick.

Detailed Description Text (12):
Covering the top surface of the wafer is an interlayer dielectric 20, which may comprise silicon dioxide. Dielectric 20 electrically insulates gate 23 from drain metalization layer 21, which covers the entire surface area of the wafer over the transistor and contacts N+ drain region 16 (except for the small area of gate contact). Interlayer dielectric layer 20 is made sufficiently thick (e.g., 1 micron) to minimize drain-to-gate capacitance for improved high frequency performance. At the same time, the large dimensions of drain metal layer 21 provide a large current conduction capability to the drain region of the device. In an alternative embodiment, drain metal layer 21 may comprise multiple layers of metal or metal alloys. In addition, drain metal 21 may be either wire bonded or soldered directly to the external package electrode.

Detailed Description Text (13):
In the on state, a sufficient voltage is applied to the gate such that a channel of electrons is formed along the surface of the P-body region 14. This provides a path for electron current flow from source electrode 22, N+ source region 17, through the channel regions formed in P-body region 14, through the N-type drift region 15, through the N+ drain region 16 and into the metal drain electrode 21.

Detailed Description Text (14):
Another embodiment of a MOSFET power device according to the present invention has opposite conduction polarity for the substrate 11, epitaxial layer 12, and deep diffusion region 19. All three regions are of the second conductivity type in this alternative embodiment. Region 14 is connected to layer 18 in another plane of view (not shown in FIG. 2).

Detailed Description Text (15):
FIG. 3 illustrates another embodiment of a MOSFET power device 30 in accordance with the present invention. In this embodiment the extended drain region 35 is connected to the N+ substrate 31 via deep N+ diffusion region 36. The N+ substrate region 31 is highly doped to achieve a low resistance path to the drain electrode and has a resistivity of about 0.005 to 0.001 ohm-cm. The metalization on the bottom of the wafer forms the drain electrode 42. The P-type or N-type epitaxial layer 32 is about 3-5 microns thick and doped to about 1.times.10.sup.16 cm.sup.-3. The P+ region 39 is included to provide a low resistance connection between region 34 and source metal 41. Both regions 34 and 39 are approximately 0.5 to 1.0 microns deep.

Detailed Description Text (16):
In this configuration the source metal layer 41 covers the top of the device and connects to source region 37 and P+ region 39 either directly or through a barrier metal, depending on the type of metalization utilized. For example, WSi is an effective barrier for Al alloy metal. The source metal layer 41 covers the top of the wafer in a contiguous manner. Insulated gate is disposed over P-type region 34 extending from source region 37 to extended drain region 35. Interlayer dielectric

Refine Search

Search Results -

Terms	Documents
L10 and (shield or sheilding)	3

Database:

US Pre-Grant Publication Full-Text Database
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EPO Abstracts Database
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IBM Technical Disclosure Bulletins

Search: L11

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Search History

DATE: Monday, October 18, 2004 Printable Copy Create Case

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L10	L9 and (isolated or isolation)	14	L10
L9	L6 and overlapping	14	L9
L8	L6 and LDMOS	0	L8
L7	L6 and DMOS	1	L7
L6	L5 and (second near3 (drain))	54	L6
L5	L4 and gate and (n adj type) and (p adj type)	103	L5
L4	L3 and (second adj conductivity)	134	L4
L3	L2 and (silicide)	499	L3
L2	L1 and (upper adj surface)	1189	L2
L1	(mos adj device)	7828	L1

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Search Results - Record(s) 1 through 3 of 3 returned.

1. Document ID: US 5663584 A

L11: Entry 1 of 3 File: USPT Sep 2, 1997

US-PAT-NO: 5663584
DOCUMENT-IDENTIFIER: US 5663584 A

TITLE: Schottky barrier MOSFET systems and fabrication thereof

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

2. Document ID: US 5229307 A

L11: Entry 2 of 3 File: USPT Jul 20, 1993

US-PAT-NO: 5229307
DOCUMENT-IDENTIFIER: US 5229307 A

TITLE: Method of making extended silicide and external contact

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

3. Document ID: US 4868617 A

L11: Entry 3 of 3 File: USPT Sep 19, 1989

US-PAT-NO: 4868617
DOCUMENT-IDENTIFIER: US 4868617 A

TITLE: Gate controllable lightly doped drain mosfet devices

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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Terms	Documents
L10 and (shield or sheilding)	3

Display Format: TI Change Format

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L11: Entry 1 of 3 File: USPT Sep 2, 1997

DOCUMENT-IDENTIFIER: US 5663584 A
TITLE: Schottky barrier MOSFET systems and fabrication thereof

Abstract Text (1):
(MOS) device systems-utilizing Schottky barrier source and drain to channel region junctions are disclosed. Experimentally derived results which demonstrate operation of fabricated N-channel and P-channel Schottky barrier (MOSFET) devices, and of fabricated single devices with operational characteristics similar to (CMOS) and to a non-latching (SRC) are reported. Use of essentially non-rectifying Schottky barriers in (MOS) structures involving highly doped and the like and intrinsic semiconductor to allow non-rectifying interconnection of, and electrical accessing of device regions is also disclosed. Insulator effected low leakage current device geometries and fabrication procedures therefore are taught. Selective electrical interconnection of drain to drain, source to drain, or source to source, of N-channel and/or P-channel Schottky barrier (MOSFET) devices formed on P-type, N-type and Intrinsic semiconductor allows realization of Schottky Barrier (CMOS), (MOSFET) with (MOSFET) load, balanced differential (MOSFET) device systems and inverting and non-inverting single devices with operating characteristics similar to (CMOS), which devices can be utilized in modulation, as well as in voltage controled switching and effecting a direction of rectification.

Brief Summary Text (2):
The present invention relates to Metal Oxide Semiconductor (MOS) device systems and procedures for fabrication thereof. More particularly, the present invention comprises single semiconductor type, Schottky barrier junction inverting and noninverting single devices which demonstrate operational characteristics similar to Complimentary Metal Oxide Semiconductor (CMOS) multiple device systems, and Schottky barrier junction voltage controlled switches which demonstrate operational characteristics similar to a nonlatching silicon controlled rectifier. In addition the present invention is, in part, a system utilizing insulator effected, channel end located, minimized Schottky barrier junction area, low leakage current Schottky barrier rectifying junction geometries in Intrinsic, N and/or P-Type semiconductor, preferably in a single substrate, to form Complimentary Metal Oxide Semiconductor Field Effect Transistor (CMOS) device systems, as well as N or P-channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices with (MOSFET) loads, and N or P-channel balanced differential (MOSFET) device systems. The present invention utilizes both rectifying and semiconductor doping and the like effected non-rectifying Schottky barrier junctions.

Brief Summary Text (5):
Briefly, a conventional (MOSFET) is comprised of N or P-type semiconductor substrate, in the surface region of which are formed regions of oppositely doped material, separated by a distance therebetween in said semiconductor substrate. The regions of oppositely doped material are termed the "Source" and "Drain" and the distance therebetween is termed the "Channel Region". Diffused rectifying junctions are thus caused to exist at the ends of the channel region, both at the source and at the drain. Continuing, atop the channel region surface is present an insulating material, such as silicon dioxide, atop of which insulating material is present a "Gate" which is made from an electrically conductive material. Application of a voltage from the drain-to-source of a proper polarity, simultaneous with the

application of a gate-to-source voltage of a proper polarity causes the channel region to "invert" and become of a doping type similar to that in the source and drain regions, thereby providing a conductive pathway between said drain and source. That is, application of a gate-to-source voltage modulates the conductivity of, hence flow of current between, the drain and source. Because the resistivity of the insulating material is high, very little gate current is required to effect modulation of said drain to source current flow. As mentioned above, conventional (CMOS) device systems comprise a seriesed combination of electrically connected N and P-channel (MOSFET) devices, formed on P and N-type semiconductor respectively. To form (CMOS) the drain of an N-channel (MOSFET) device is electrically connected to the drain of the a P-channel (MOSFET) device and the source of the P-channel device is connected to a positive (+Vdd), while the source of the N-channel (MOSFET) device is connected to a lower voltage (-Vss), typically ground. In use, a relatively low, (approximately the voltage appplied to the source of the N-channel (MOSFET) device), gate voltage applied simultaneously to the gates of said electrically connected devices modulates the P channel device so that it conducts, while having no channel conductivity increasing effect on the N channel device. Similarly, simultaneous application of a relatively high, (with respect to the voltage applied to the source of the N-channel (MOSFET) device, eg. approximately +Vdd), gate voltage affects the N and P channel devices in an opposite manner. That is the N-channel device channel inverts and conductivity is effectively increased from the associated source to drain, while the P-channel device channel conductivity is not increased. The result being that varying gate-to-source voltage from relatively low, (-Vss), to relatively high, (+Vdd), causes the voltage present at the electrically connected N and P-channel device drains, which terminal is essentially electrically isolated from the gates, to vary essentially between that applied to the source of the P-channel device, (+Vdd), and that applied to the source of the N-channel device, (typically, but not necessarily, ground potential), respectively. Said (CMOS) is then inverting between input and output. As mentioned above, (CMOS) switching is effected with very little gate current flow, as the insulating material between the gate and the semiconductor is of a very high resistance, (eg. ten-to-the-forteenth ohms or higher). As well, drain to source current flows only briefly at the switching point when both devices are momentarily conducting. This is because current cannot flow through an electrically connected series of (MOSFETS) when either thereof does not have a conducting inverted channel present. Conventional (MOSFET) and (CMOS) operational characteristics are described in numerous circuit design texts such as "Basic Integrated Circuit Engineering" by Hamilton and Howard, McGraw-Hill; 1975.

Brief Summary Text (10):
A Search of relevant references has provided an article by Hogeboom and Cobbold, titled "Etched Schottky Barrier (MOSFETS) Using A Single Mask". Said article describes the fabrication of a P-Channel (MOSFET) on N-type silicon with aluminum forming the rectifying junction schottky barrier source and drain junctions. (Note that aluminum does not form a rectifying junction schottky barrier on P-type silicon hence is not an appropriate metal for use in realization of N-channel Schottky barrier (MOSFETS)). Said article also describes both N and P-Channel conventional diffused junction (MOSFETS) fabricated using a single mask, but which required a diffusion of a dopant, hence, did not operate based upon schottky barrier junction presence. Aluminum present provided non-rectifying contact to diffused regions as in conventional (MOSFETS). This paper also suggests the use of vanadium to form source and drain regions. It is also noted that this paper describes use of a silicon dioxide undercutting etch which facilitates self delineation of fabricated devices when essentially line-of-sight aluminum deposition is achieved. (The silicon etchant taught is a mixture of fifty (50) parts acetic acid, thirty (30) parts nitric acid, twenty (20) parts hydrofluoric acid and one (1) part aniline). A Patent to Welch, U.S. Pat No. 4,696,093 describes a procedure for fabricating Schottky barrier (MOSFETS), including an approach requiring only one-mask and one-etch and the use of chromium, (which after application to silicon is subjected to an annealing procedure to form chromium

disilicide), as the metal used to form rectifying source and drain Schottky barrier junctions. A Masters Thesis presented by James D. Welch at the University of Toronto in 1974 titled "Design and Fabrication of Sub-Micron Channel MOS Transistors by Double Ion-Implantation" mentions Schottky barrier rectifying junctions discovered to exist after a thirty (30) minute, six-hundred-fifty (650) degree centigrade anneal of chromium present on the back, unpolished, side of an N-type silicon substrate. The reverse breakdown voltage of said rectifying junctions was found to be upwards of eighty (80) volts. However, said thesis work did not include investigation of annealing deposited chromium on P-type silicon. A paper by Lebedev and Sultanov, in Soviet Physics Semiconductors, Vol. 4, No. 11, May 1971, pages 1900-1902 teaches the chromium diffused into P-type Silicon at high, (eg. twelve hundred (1200) degrees centigrade), for long periods of time, (eg. twenty (20) to fifty (50) hours), dopes said P-type silicon N-type. Nothing, however, is stated regarding the properties of chromium disilicide formed by annealing a thin film of chromium which has been deposited upon said P-type silicon silicon at lower temperatures. A paper by Lepselter and Sze, titled "SB-IGFET: An Insulated-Gate Field Effect Transistor Using Schottky Barrier Contacts for Source and Drain", in the Proceedings of the IEEE, August 1968, pages 1400 through 1402 describes a P-Channel schottky barrier insulated gate field effect transistor, (ie. IGFET), fabricated using schottky barrier junctions for source and drain. Said IGFET utilized platinum silicide in the formation of the source and drain junctions. It is stated that during operation the source junction of the device is reverse biased in the inverted channel region and that reverse leakage or tunneling current therethrough is what applied gate voltage modulates. The Lepselter et al. article however, makes no mention of the use of Schottky barriers to form N-Channel devices on P-type silicon. In fact, owing to the rather large reverse barrier height difference between platinum silicide and N-type silicon, (ie. 0.85 ev), and between platinum silicide and P-type silicon, (ie. 0.25 ev), it is unlikely that N-channel devices would be operablle, or even if they were, that an effective (CMOS) device system could be achieved using platinum-silicide to form both N and P-channel devices. This is because the (MOSFET) devices in a (CMOS) device system must have essentially symetrical and complimentary operational characteristics to provide efficient switching capability. The Lepselter et al. article provides an equation for calculating tunneling current density through a reverse biased Schottky barrier junction: ##EQU1## where E is the electric field induced by application of a voltage across the junction,

Brief Summary Text (16):
Continuing, a recent Patent to Honma et al., U.S. Pat. No. 5,177,568 describes a tunnel injection type semiconductor device having a Metal-Insulator-Silicon (MIS) structure comprising a semiconductor region, a source, a drain and a gate electrode wherein said source and drain are composed of a metal or metal compound member, respectively, and wherein both have an overlapping portion with said gate electrode. The Source provides a Schottky barrier junction to said semiconductor region while said drain provides an non-rectifying contact to said semiconductor region. A tunneling current is caused to flow across a Schottky barrier junction between said source and said drain, controlled by a gate voltage. This Patent describes formation of a (CMOS) device system wherein schottky barriers serve as source region contacts to N and P-type silicon and wherein interconnected drain contacts are non-rectifying. The devices described in this Patent are very interesting, but fabrication thereof obviously requires rather complicated channel region doping profile effecting and yield reducing steps to effect rectifying junctions at the source and non-rectifying junctions at the drain of a (MOSFET) structure. That is, economic savings as compared to conventional diffused junction (MOSFET) fabrication would seem to be reduced by the channel doping requirements. Use of doping and varying band gap materials are disclosed as approaches to realizing the device described. It is also noted that the devices described apparently operate, (show gate controlled drain current flow), with the semiconductor between source and drain "accumulated" while a source Schottky barrier junction is reverse biased by applied drain to source voltage polarity.